REMARKS

Claims 17-22 were pending and rejected under Section 102 in view of Totsuka (USP 6,715,090) and under Section 103 in view over Uchiyama (USP 6,748,507) in view of Totsuka. Applicant acknowledges with thanks the withdrawal of the rejection under Section 112.

While Applicant respectfully traverses the rejections in view of Totsuka and Uchiyama, Applicant has chosen to refine the claimed subject matter via the newly-submitted claims. Claims 17-22 have been canceled.

First, Applicant notes that the present invention, as defined in the presently-submitted claims, recites an external interface module outputting a control signal for controlling an external synchronous memory, and the microprocessor/microcomputer outputs a clock signal. The CPU is operable to access the external interface module for accessing the external synchronous memory. As recited in the claims, a graphics processing module, three-dimensional image processing accelerator and/or direct memory access controller also are provided in combination. It is submitted that such features are distinguishable from the cited references.

All rejections were based in whole or part on Totsuka. Totsuka, however, is not prior art to the present application. The present application claims priority to the ultimate parent application, serial no. 08/306,100, filed on September 14, 1994. Totsuka has a PCT filing date of November 21, 1997 (claiming priority to a Japanese application filed November 21, 1996). Applicant submits that, based on the priority claim of the present application, Totsuka is not prior art to the present application and the rejections should be withdrawn.

Moreover, Uchiyama also is distinguishable from Applicant's invention. Uchiyama does not disclose or suggest, for example, the microprocessor/microcomputer outputting a clock signal that is provided external to the microprocessor/microcomputer for controlling an external synchronous memory, particularly as claimed by Applicant in combination with the other recited features such as the graphics processing module, three dimensional image processing accelerator, etc. See, e.g., MPU 101, MS 102, MC 104 and CG 103 of Uchiyama Fig. 1 and related description. Uchiyama discloses a different arrangement from that described and claimed by Applicant.

Accordingly, Applicant submits that the presently pending claims are distinguishable over the cited references and allowance is requested.